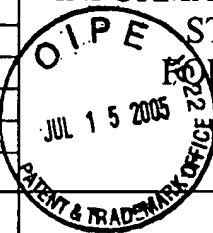


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Examiner Name	Tu Tu V. Ho	
Allowed	April 28, 2003	
Confirmation No.	9673	
Attorney Docket No.	400.264US01	
Title: 4F2 EEPROM NROM MEMORY ARRAYS WITH VERTICAL DEVICES		Sheet 1 of 2

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